Smart Clocks Simplify 4G Timing Design

As next generation technologies develop, demand for extremely accurate timing sources with tight tolerances is no longer a luxury.

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Emerging 4G networks rely on precision timing references to provide synchronization across heterogeneous infrastructures such as internet protocol (IP), synchronous optical network (SONET), synchronous digital hierachy (SDH), asynchronous transfer mode (ATM), CDMA2000, wide code-division multiple access (WCDMA), universal mobile telecom service (UMTS), and time-division multiple access (TDMA). Accurate clocks, with resolution as low as 1ns are needed for synchronizing multiple diversified Stratum 1 references such as global positioning systems (GPS), Cesium, CDMA, LORAN-C, and E1/T1 network span. This is important both for high-availability systems that can switchover from one master to another, should the first source fail; and for developing versatile designs that can be used with alternative reference clocks. In a wireless environment, poor synchronization generates dropped calls. For designers, the challenges and complexities of system engineering that can receive such a diversity of timing references are clear.

New developments in integrated, synchronized multi-reference clocks are helping designers create more versatile solutions, reducing development time and effort by design risk and system cost.

First-generation Rubidium or crystal oscillators were simple frequency sources for which the complex timing and disciplining functions had to be designed separately and specifically by engineers for each reference type (See Figure 1). For instance, for a clean Cesium reference, an oscillator needs to follow the long-term stability of its reference as closely as possible. The disciplining resolution is the limitation of how well the oscillator can follow its reference. Conversely, for a noisy GPS reference, an oscillator needs to filter its reference as much as possible to mitigate the noise while following the long-term stability of its reference. Key functions had to be implemented externally on costly, separate circuit boards.

Next-generation technologies like the smart SynClock eliminate these disadvantages by providing a compatible, plug-and-play environment, in which any type of reference can be seamlessly interconnected and auto-adaptively disciplined, regardless of the oscillator type.

What to Look for in Smart Clocks

Designers seeking these benefits should look for devices that intelligently synchronize, discipline, and control multiple types of reference at cutting-edge nanosecond resolution.

One key requirement for GPS application is a multi-vendor GPS interface offering auto-adaptive reference filtering, disciplining, control, and time RAIM/Position hold signal optimization. Four G clock designers' wish lists should also include the capability for auto-adaptive reference disciplining and jitter/wander/noise filtering between 0 and 100,000 at 1 ns resolution, exceeding standard specifications such as I-95 CDMA, and calling for either <10 µs/24 hours or <10 µs/48 hours holdover, UMTS/WCDMA, calling for <50 ns frequency offset, and MTIE/TDEV G.823 & 824/T1.101 & 102 standards for T1/E1 reference.

Additionally, these devices must offer auto-adaptive frequency stability over fast temperature changes at 0.1°C resolution across the operational temperature range.

In scanning the market for available options, designers should critically assess the range of programmable features to simplify configuration, adjustment, monitoring and performance testing of their smart clock system. Can 1PPS output phase/time offset be adjusted between 0 and 1 s? Does it provide the options to choose sync or track modes using either hardware or software: that is, to either time/phase align 1 pps output from a 1 pps GPS reference through the sync mode or to frequency track 1PPS output from a 1 pps GPS reference through the Track mode? Does it need external memory to store, upgrade and back up data?

Features that Bind

Built-in electronically eraseable programmable read-only memory (EEPROM) will allow engineers to make TIE performance measurements, auto calibrate frequency and back-up settings in case of power failure. They will also help to future-proof the application by providing seamless software upgrades.

Connection, set-up, evaluation and monitoring are typically achieved through a standard RS-232 communication interface. User-friendly American standard code for information exchange (ASCII) commands will ease control, configuration, fault, and performance management.

Climbing the Learning Curve

Manufacturers' design kits facilitate evaluation using the last of these options. Such kits enable users to quickly test the performance of the on-board SynClock and interconnect the design kit to their system to validate design concepts.

Most kits today include software that allows PCs to communicate with the

devices. For this particular case, GPS configuration can be set up from the iSyncManager software. The PC serial link is then detached and the smart clock connected directly to the GPS module output. Hardware SYNC and track switches are provided on the development kit. Pressing the reset button automatically configures the GPS. Then, reconnecting the PC after a power-down cycle allows designers to use the design kit software to initiate tracking and synchronization, and check its operation.

The evaluation kit guides designers through the setup of the device as a free-running oscillator, either using variable voltage or impedance to adjust frequency in hardware, or using another 10 MHz master and high-resolution frequency counter to make the appropriate adjustments in software.

When operating as a tracking oscillator, the software provides facilities to check and measure tracking performance, either through simple observation of status flags, or by displaying the phase difference and tracking frequency. Tracking loop time constants, normally set automatically after analyzing the stability of the reference, can be forced via software. One example is when there is a requirement to quickly reach the frequency of a master oscillator. In unforced mode, it is possible to measure the time constant that has been set automatically.

Designers can also study the effect of changing frequency-save parameters. By default, the average tracking frequency is saved to EEPROM every 24 hours, but the reference frequency can alternatively be stored on demand, either as an average since the last save or as a snapshot of the actual current frequency.

By using the design kit to measure the phase difference between the clock and its reference, further parameters can be set to ensure that the SynClock consistently tracks a master at least as stable as itself. Designers can adjust phase error limit settings, to ensure that warning alarms are displayed correctly and that tracking stops when it should.

Oscilloscope experiments provide further evaluation options. For example, in free-running mode, scope measurements can be used to study how the PPS OUT pulse moves when delay is changed. In tracking mode, they can be used to confirm that delay is referenced to the source when tracking is perfect.

Similar measurements can be made to confirm the correct operation of Sync mode. In particular that the clock has both frequency and PPS phase or time aligned to those of the master.

Lastly, attaching a counter and master reference to the clock allows still more detailed analysis of system performance.

SmarTiming+ Disciplining Performance

Figure 2 illustrates the disciplining performance of the device technology used inside the device. Depending on the noise level or quality of the GPS signal and the environmental temperature variation, which influences the long-term stability, the device automatically adapts its loop time constant to discipline its reference while optimizing the output performance. The same concept is used when other types of reference are fed to the device — such as Cesium or E1/T1 span line with different quality or noise levels.

Smart Holdover Performance

In case of the absence of GPS reference, a free-running clock system has to maintain its timing stability as long as possible to avoid telecom service failure. This is called the holdover performance in engineering terms. It is the key specification in wireless applications, as it defines the mean time to repair (MTTR) before a base station drops all its calls. Figures 3 and 4 illustrate the extended holdover performance of the device, either configured with a Rubidium and a crystal oscillator.

Conclusion

Technologies such as smart SynClocks are simplifying the design of core timing, frequency, and synchronization for 4G applications. Designers are set to benefit from highly integrated functionality in an ultra small, single low-cost package. What is more, the availability of pin-compatible modules with a choice of Rubidium or crystal oscillators allows engineers to seamlessly design a common system platform. In this way they can efficiently address different markets having different price sensitivities.

The auto-adaptive SmarTiming+ disciplining technology provides a compatible, plug-&-play solution, eliminating the need for designing an external reference disciplining and control system for each reference type. ■

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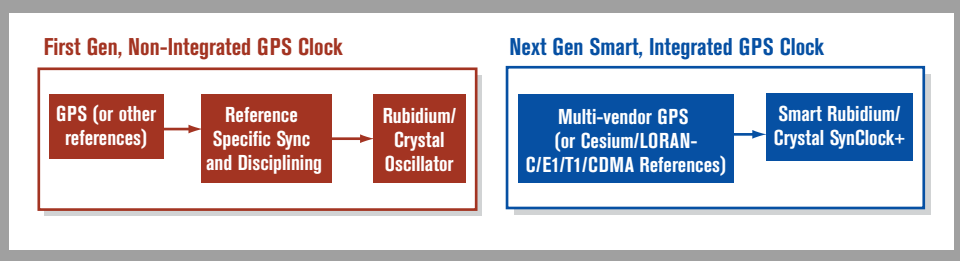

Figure 1. First vs. Next Generation GPS/Multi-Reference Clock designs

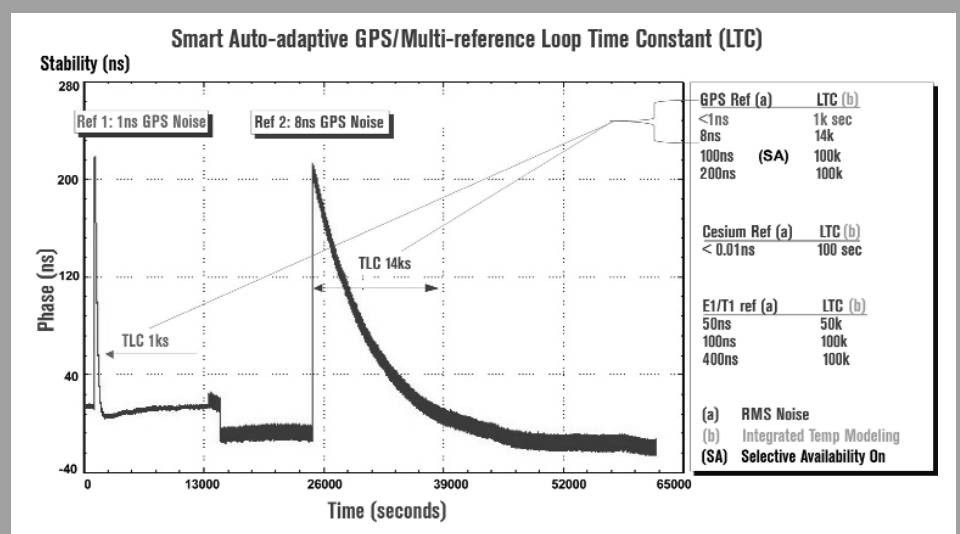

Figure 2. SmarTiming+ disciplining performance

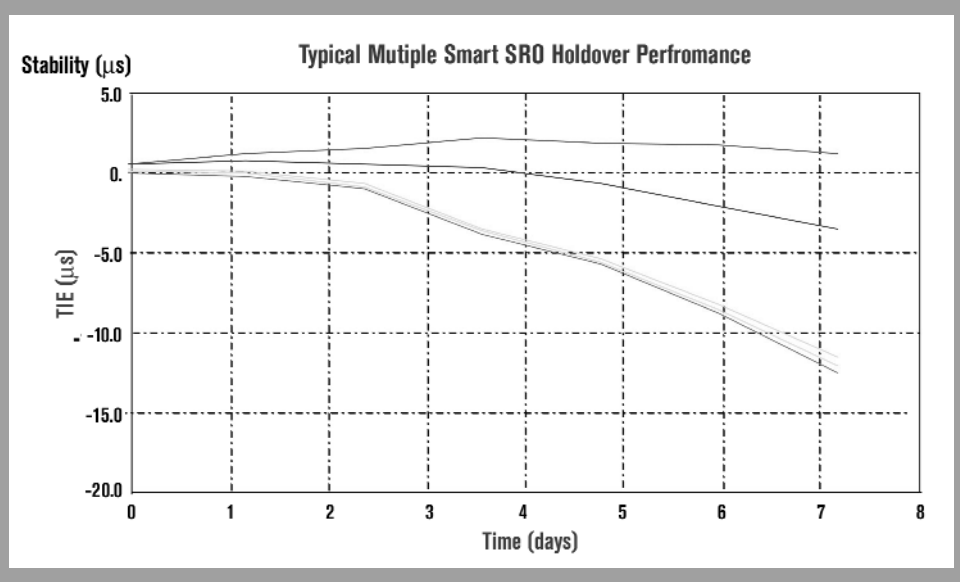

Figure 3. Smart Rubidium holdover performance

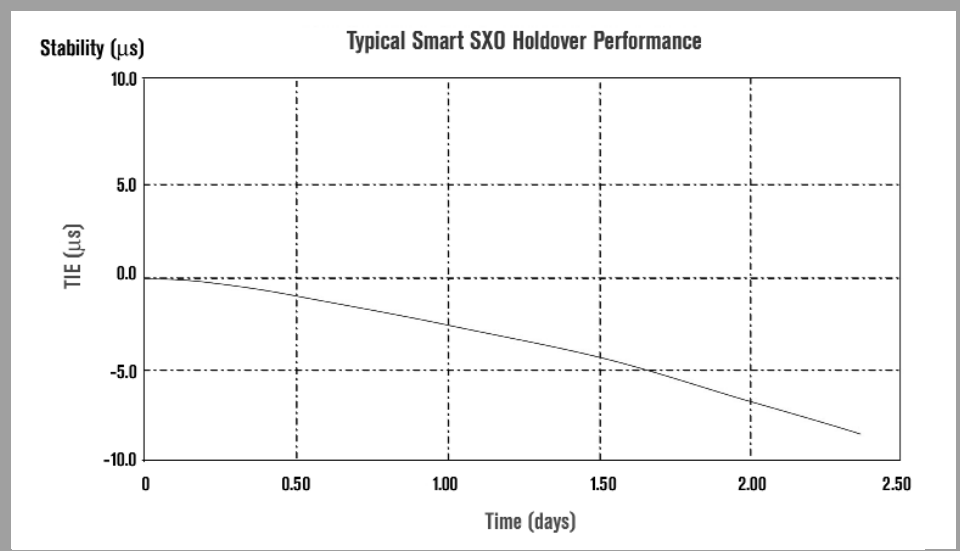

Figure 4. Smart Crystal holdover performance